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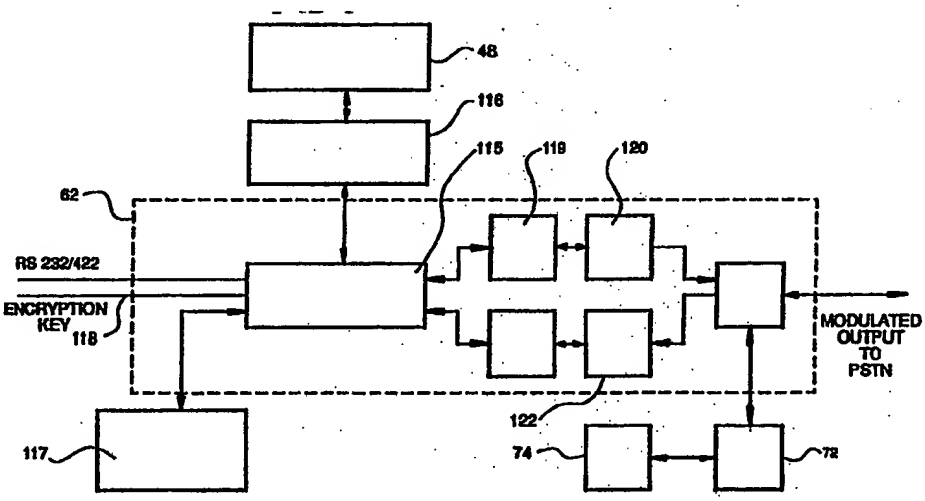
(54) Title: DIGITAL VIDEO CAMERA

(57) Abstract

A digital video camera employs an encryption means for scrambling the digital image in accordance with an encryption algorithm. The camera employs a modem and line driver circuit (62) which employs a microprocessor (115) which co-operates with a main microprocessor (48) via an interface (116). The microprocessor (115) accumulates bytes representing pixels in packets between (32) and (128) bytes whereafter the encryption algorithm is supplied to the packet before transmission of the resultant data stream. Sum bits are added to the string for the purpose of checking the integrity of the data string at the receiver and subsequent error correction if necessary. The digital video camera employs a pixel comparator (50) operating at high speed to enable a (50) frame per second throughput. The main microprocessor (48) performs software support and the control functions within its speed capabilities. The microprocessor operates in combination with the pixel comparator (50) which is hardwired. Successive frames are stored in RAMs (101) and (102) on a pixel per byte basis. The RAMs are sequentially addressed by a counter (103) so the contents of corresponding addresses are delivered to the data out lines, the data out lines of the respective RAMs are connected in order of significance to a logic discriminator having respective circuit elements (104) through (111) which each serve an exclusive-OR function to detect identity or difference between bits in order to detect movement.



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DIGITAL VIDEO CAMERA

TECHNICAL FIELD

THIS INVENTION relates to a digital video camera and in particular to an integrated camera, digital processor and modem suitable for digital communication in a surveillance system.

BACKGROUND ART

Conventional video transmission over long distance has been in analogue form employing systems which are generally expensive. The advantage of digital communication has been recognised but attempts to digitise and transmit digital images over long distances, say through the public switched telephone network (PSTN) have been commercially unsuccessful. One system involves the use of a conventional TV camera, the analogue image of which is processed through a separate A to D convertor which digitises the image and sends the digital information to a modem. The modem then generates a modulated audio signal which can be transmitted down a phone line. At the receiver, the modulated audio signal is demodulated to retrieve the digital information which is then processed through a D to A convertor after which the analogue image can be reproduced on a screen. The television camera, modems and convertors are essentially independent units which employ technology suitable for rapid transmission of text data but not suitable for rapid transmission of the much greater amount of data required for reproduction of an image. The system is bulky, expensive and slow which renders it commercially unacceptable and therefore it has not found general application.

In the security environment surveillance systems employing closed circuit television have been used to enable an operator at a central location to simultaneously monitor a number of screens, the screens each displaying images from strategically placed television cameras. The closed circuit television surveillance system is dependent on the operator and operator error can reduce the

effectiveness of the system.

Conventional alarm systems do not transmit a video image when an alarm condition is initiated and as a great proportion of alarms are false alarms, it would be desirable to provide a cost effective system capable of providing a confirmatory video image on initiation of say a fire alarm.

While it would be desirable to utilise the PSTN for transmission of video images, apart from the aforementioned problems of conventional systems, the systems do not provide for security against phone taps or other unauthorised access.

DISCLOSURE OF THE INVENTION

It is an object of the present invention to alleviate at least to some degree the aforementioned problems associated with the prior art.

In one aspect, the invention resides broadly in a digital video camera suitable for digital communication in a surveillance system, the camera including:

a) an image pick-up means for converting image information to electrical frame information;

b) storage means for storing the electrical frame information as a stored digital image;

c) a digital processor for processing the stored digital image to provide a digital image signal;

d) an encryption means for scrambling the digital image signal in accordance with an encryption algorithm; and

e) communication means for enabling communication of the encrypted digital image signal from the camera.

The image pick-up means can be any light sensitive transducer such as a charge coupled device (CCD) or a solid state detector such as a dynamic random access memory. The sensor can be sensitive to light having frequencies inside or outside the visible spectrum.

The storage means is preferably a random access memory (RAM). Advantageously, two RAMs are employed so that successive frames can be stored for comparison.

The digital processor can include a microprocessor which can be programmed to automatically perform a predetermined decision making sequence in relation to the stored digital image. Advantageously, the digital processor includes a hardwired comparator for comparing successive frames against a threshold difference value indicative of motion.

The encryption means can be provided in the form of discrete circuit element or can be implemented as software utilising any known or modified encryption algorithm technique.

The communication means preferably includes input and output modem drivers to enable higher speed transmission from the camera than to the camera. Where the camera is employed for motion detection in order to reduce the amount of data transmitted, it is preferable only to transmit those digital images which on comparison have values exceeding the threshold. In a surveillance environment it is preferable that the camera operate in conjunction with peripheral detectors such as intruder detectors or smoke detectors which can initiate operation of the camera when the detectors sense an adverse condition.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the invention can be more readily understood and be put into practical effect, reference will now be made to the accompanying drawings and wherein:

Figure 1 is a pictorial view of a camera constructed in accordance with the present invention.

Figure 2 is a schematic block diagram illustrating one embodiment of the present invention.

Figure 3 is a schematic block diagram illustrating a preferred embodiment of a hardwired comparator applicable to the present invention; and

Figure 4 is a schematic block diagram illustrating part of a preferred communication means applicable to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring to the drawings and initially to Figure 1 there is illustrated a digital video camera 10 constructed in accordance with the present invention.

Figure 1 serves to illustrate the compact construction of the camera which in this embodiment employs a charge coupled device housed behind the lens 12 with the electronics being housed in a compact housing 13. Figure 2 illustrates the internal elements 11 of the camera of Figure 1 and as can be seen, the camera includes an image pick-up means which in this case is a CCD 40, a storage means in the form of a memory module 46, communication means in the form of RS232/422 driver 60, modem and line drivers 62, buffer 64 for a digital TTL output and a local alarm output from digital output drivers 66. In the illustrated embodiment the communication means also includes buffers and multiplexers 68 for input of data from external peripherals such as smoke detectors and auxiliary cameras. The signal delivered to the modem 62 from the microprocessor 48 is encrypted before being transmitted (this will be described further having regard to Figure 4). The CCD 40 provides its analogue output to vertical/horizontal separator 42 before being fed to analogue to digital converter 44. The memory module 46 stores the digitised value of the image from CCD 40. The microprocessor 48 communicates with memory 46 via bus 47. This memory module 46 stores at least two frames of the image for processing by pixel comparator circuitry 50. The image of two successive frames are fed to pixel comparators 52 and 54 respectively. These comparators 52 and 54 can compare the image on an individual pixel, line or block basis providing a tally in counters 56 and 58. The result of these comparisons can then be stored in the microprocessor 48 during the horizontal and/or vertical blanking intervals. Under the control of microprocessor 48 motion detection and adjustment of the parameters controlling the sensitivity of the comparison for ambient

lighting conditions are performed.

The pixel comparator 50 operates at high speed to enable a 50 frame per second throughput. Thus it operates in real time freeing the microprocessor 48 to perform software support and the control of functions within its speed capabilities. This combination of hardware comparator 50 and microprocessor 48 provides a real time image processing environment at the camera. The microprocessor 48 performs calculations based on the parameters chosen for allowable pixel, line, or block changes as the case may be. These parameters are under software control as well as external control (via buffers and multiplexers 68).

If the microprocessor 48 detects a relevant condition e.g. movement indicating intrusion in a security environment, the microprocessor 48 can signal this fact to the external world via RS232/422 drivers 60, modem 62, buffers 64 providing a TTL (Transistor Transistor Logic, or +5V logic '1') output or output drivers 66 signalling a local alarm output. These output devices can signal the detection of an alarm condition and/or send the image as a digital output. The camera output can also be provided as an analogue signal from line 61.

The output signal can then prompt an external device (see Figs. 5, 7 or 8) to communicate with the intelligent camera via buffers and multiplexers 68. These buffers 68 can also provide input from other sensors such as smoke detectors, pressure or contact switches, or other image sensors.

The microprocessor 48 can also control the auto dial circuitry 70 to dial up the relevant emergency utility in the event of a fire or intrusion detection.

The camera can also be provided with voice circuit 72 which provides acoustic input or output from loudspeaker and microphone 74. This acoustic input/output can be processed by microprocessor 48, for example, to detect a person's presence in a fire or input/output directly via

the modem 62 to provide two way contact.

Referring to Figure 3 there is illustrated the operation of a typical pixel comparator 100. In the illustrated embodiment, successive frames are stored in RAMs 101 and 102 on a pixel per byte basis. The RAMs are sequentially addressed by counter 103 so the contents of corresponding addresses are delivered to the data out lines. The data out lines of the respective rams are connected in order of significance to a logic discriminator having respective circuit elements 104 through 111 which each serve an exclusive - OR function to detect identity or difference between bits. Element 104 has an output representing a comparison between the respective least significant bits whereas the output from 111 represents a comparison between the most significant bits. Thus for any comparison between two 8 bit bytes there are 256 possible variations. The outputs from elements 104 to 111 are fed to a memory buffer/comparator circuit 112 which includes a stored threshold value for comparison with the output from the logic discriminator. The threshold value is loaded into memory buffer 112 and the comparison is made as the output from the elements 104 through 111 is loaded into the memory buffer 112. The threshold value represents the desired sensitivity for the comparison and in most cases only the more significant bits are compared. For example, for low sensitivity, the outputs from elements 109, 110, 111 need be the only relevant outputs for the comparison. If greater sensitivity is required additional outputs can be involved. When the threshold is exceeded, a 1 is set at the output 113 to initiate further operations of the microprocessor 48. The threshold value is loaded into memory buffer 112 along line 114 when the microprocessor is programmed. Once the threshold is exceeded further comparison is not required and the frame can be transmitted to the receiver. If the comparison gives a negative result there is no need to send the frame and the preceding frame can be maintained at the receiver if need be.

Referring to Figure 4, there is illustrated the operation of a preferred modem and line driver circuit 62 applicable to the present invention. The circuit 62 includes a microprocessor 115 which co-operates with microprocessor 48 via an interface 116.

As data for transmission is delivered to microprocessor 115 from microprocessor 48 it is processed by microprocessor 115 to scramble the data using an encryption circuit 117. The encryption algorithm can be a modified Data Encryption Standard (DES) which includes a unique encryption key programmed along line 118. While encryption can be implemented using hardware the encryption algorithm can be implemented using software in known fashion. In the present case, the microprocessor 115 accumulates bytes representing pixels in packets of between 32 and 128 bytes whereafter the encryption algorithm is applied to the packet before transmission of the resultant data string. Sum bits are added to the string for the purpose of checking the integrity of the data string at the receiver end and subsequent error correction if necessary.

The encrypted signal is then passed from the microprocessor 115 to a buffer 119 before being modulated by the V29 modem driver 120 after which the 9600 baud signal passes through the line interface 12 and is transmitted. As more data is transmitted, incoming data is processed at a slower speed through a back channel operating at 1200 baud via V23 modem driver 122, buffer 123 and to microprocessor 115 for subsequent forwarding of the commands to microprocessor 48.

Whilst the above has been given by way of illustrative example of the present invention, many modifications and variations will be apparent to persons skilled in the art without departing from the broad ambit and scope of the invention as set forth in the appended claims.

CLAIMS

1. A digital video camera suitable for digital communication in a surveillance system, the camera including:-

(a) an image pick-up means for converting image information to electrical frame information;

(b) storage means for storing the electrical frame information as a stored digital image frame;

(c) a digital processor for processing the stored digital image frame to provide a digital image signal;

(d) an encryption means for scrambling the digital image signal in accordance with an encryption algorithm; and

(e) communication means for enabling communication of the scrambled digital image signal from the camera.

2. A digital video camera according to claim 1 wherein the storage means employs memories so that successive image frames can be stored and the digital processor includes a hardwired comparator for comparing the successive image frames against a threshold difference value indicative of motion.

3. A digital video camera according to claim 2 wherein the comparator comprises a logic discriminator to provide an output indicative of identity or difference between bits stored in the memories and a threshold comparator for comparing the output from the threshold comparator with a threshold difference value.

4. A digital video camera according to claim 3 wherein the logic discriminator comprises a plurality of exclusive-OR circuits having respective inputs from the respective memories for comparing the contents of the memories on a bit by bit basis.

5. A digital video camera according to any one of the preceding claims wherein the encryption means comprises a modem and line driver circuit including a second digital processor interfaced with the first mentioned digital processor means for scrambling the digital image signal.

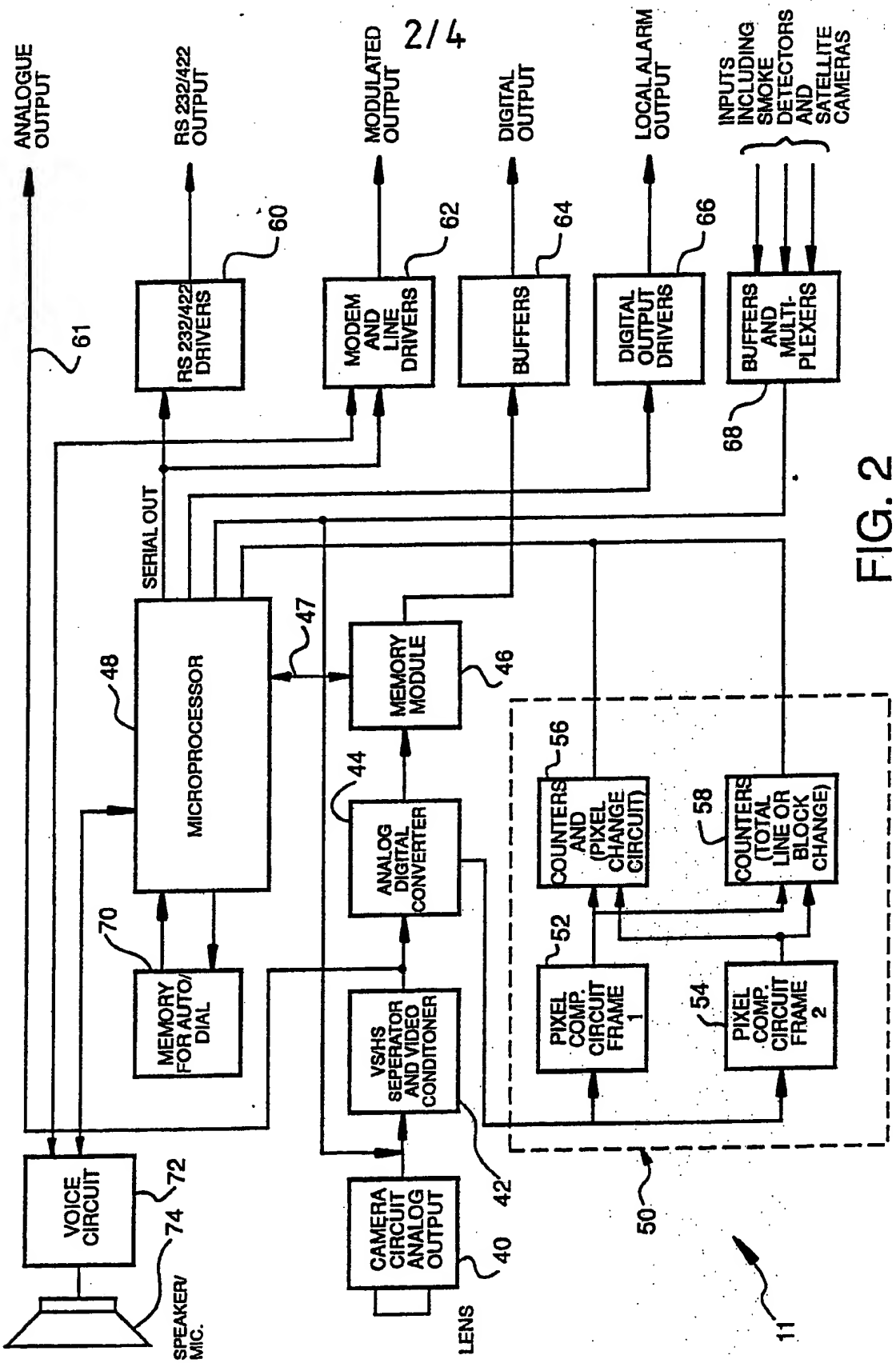
ANALOGUE OUTPUT
RS 232/422 OUTPUT
MODULATED OUTPUT
DIGITAL OUTPUT
LOCAL ALARM OUTPUT
INPUTS INCLUDING SMOKE DETECTORS AND SATELLITE CAMERAS
61
60
62
64
66
68
RS 232/422 DRIVERS
MODEM AND LINE DRIVERS
BUFFERS
DIGITAL OUTPUT DRIVERS
BUFFERS AND MULTI-PLEXERS
SERIAL OUT
47
48
MICROPROCESSOR
MEMORY MODULE
46
44
ANALOG DIGITAL CONVERTER
56
COUNTERS AND (PIXEL CHANGE CIRCUIT)
58
COUNTERS (TOTAL LINE OR BLOCK CHANGE)
70
MEMORY FOR AUTO DIAL
52
PIXEL COMP. CIRCUIT FRAME 1
54
PIXEL COMP. CIRCUIT FRAME 2
VS/HS SEPERATOR AND VIDEO CONDITONER
42
VOICE CIRCUIT
72
74
CAMERA CIRCUIT ANALOG OUTPUT
40
50
SPEAKER/ MIC.
LENS
11

FIG. 2

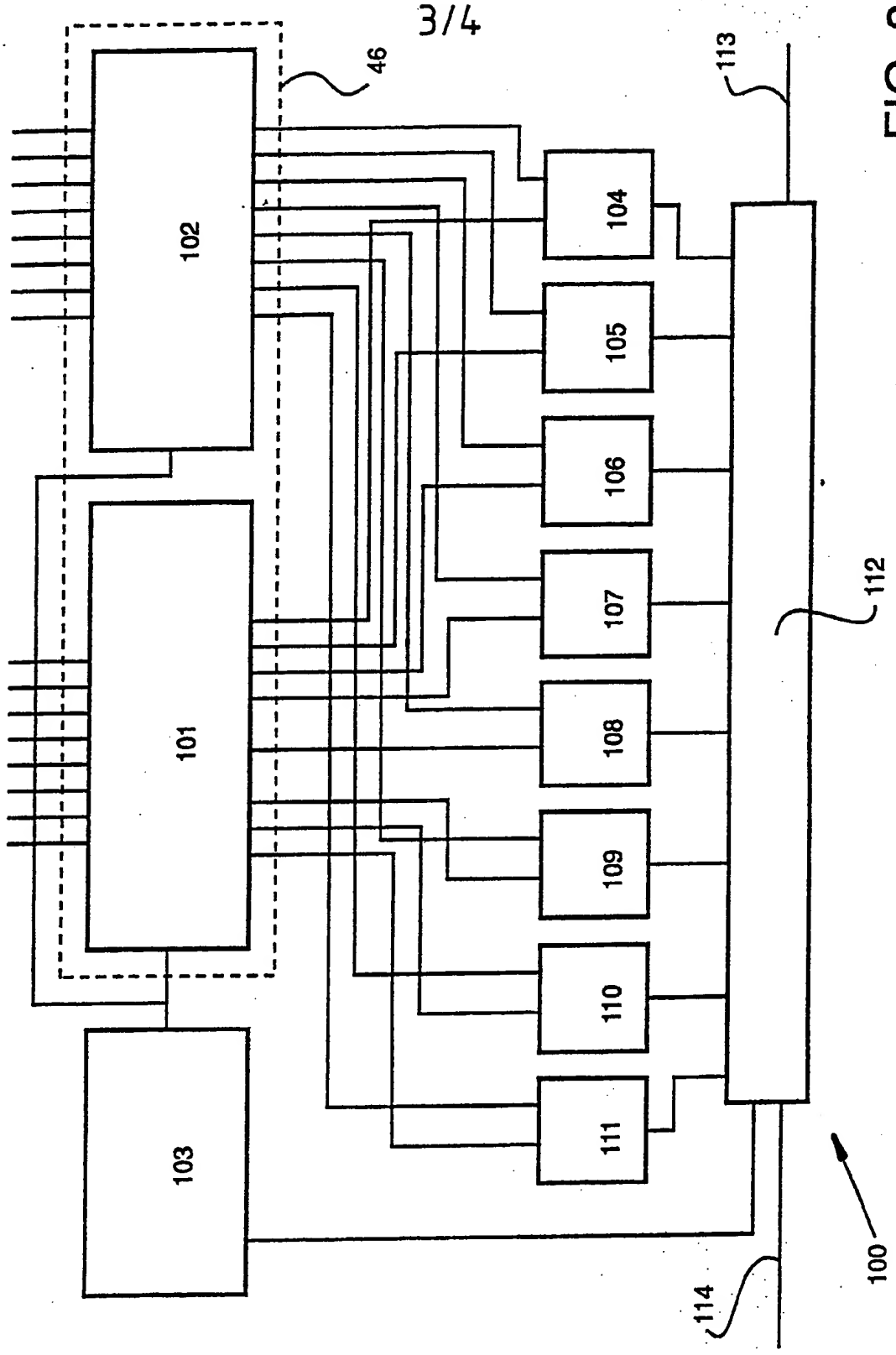

FIG. 3

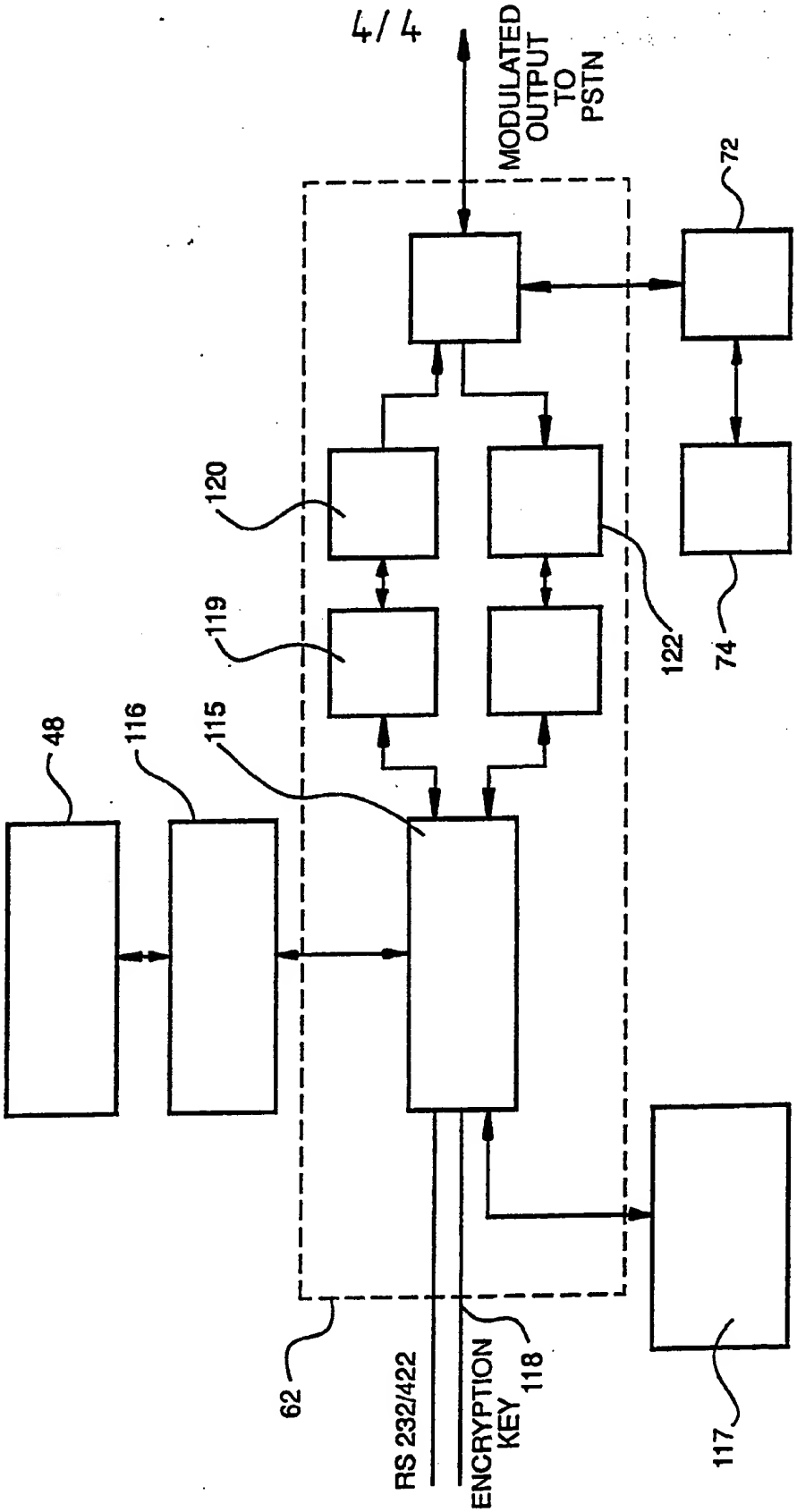
MODULATED OUTPUT TO PSTN
72
120
119
122
74
48
116
115
62
RS 232/422
ENCRYPTION KEY
118
117

FIG. 4

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 6

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[5] H04N 7/18

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
IPC	H04N 7/18

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 8

AU : IPC as above; Australian Classification 05.42

III. DOCUMENTS CONSIDERED TO BE RELEVANT 9

Category*	Citation of Document, 11 with indication, where appropriate, of the relevant passages 12	Relevant to Claim No 13
Y	EP,A, 291036 (MEDAON LTD) 17 November 1988 (17.11.88) See Fig 1, column 1 line 1 to column 2 line 15	(1,5)
Y	EP,A, 304217 (YEDA RESEARCH AND DEVELOPMENT COMPANY, LTD) 22 February 1989 (22.02.89) See page 2 line 13 to page 3 line 45	(1,5)
Y	EP,A, 339948 (UVC CORP) 2 November 1989 (02.11.89) See column 1 line 9 to column 4 line 41	(1,5)
Y	US,A, 4458266 (MAHONEY) 3 July 1984 (03.07.84) See Fig 1, column 3 line 21 to column 4 line 63	(1,2,3)
A	US,A, 4774570 (ARAKI) 27 September 1988 (27.09.88) See column 1 lines 9 to 16, column 2 line 19 to column 4 line 68	

* Special categories of cited documents: 10

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
6 February 1991 (06.02.91)	20 February 1991
International Searching Authority	Signature of Authorized Officer
Australian Patent Office	P.P. GERONDAL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON
INTERNATIONAL APPLICATION NO. PCT/AU 90/00541

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Members		
EP 291036	AU 16106/88 ZA 8803293	IL 82539	US 4945404
EP 304217	AU 20671/88 US 4910772	IL 83549	JP 1157686
EP 339948	AU 33542/89 US 4914508	FI 896255 WO 8910673	IL 90025 US 4857993
US 4458266	AU 77221/81 DE 3175493 JP 63060960	AU 537554 EP 62655 WO 8201454	CA 1172746 JP 57501907
US 4774570	EP 261917	JP 63077284	JP 63077285

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